**EENG 5560**

**ASSIGNMENT 2**

**Assigned – February 9, 2023**

**Due – February 16, 2023**

* 1. Design a fully connected 2x2 reconfigurable computing architecture where each computational unit (CU) in a row can send information to any of the CUs in the row below it. For example, CU(1,1) can send information to CU(2,1) and CU(2,2). Each CU can perform Addition, Subtraction, Multiplication, Greater Than, Less Than and Equal to operations.
* Use Xilinx Vivado to design and simulate the logic shown above.
* Inputs are 4-bit wide.
* Make sure you test your design for all the operations listed above.

Submit vhdl code, RTL schematic, screenshots of simulation waveforms, and test bench of the design. Test your design using at least five test cases. Mark two of the test cases and show the corresponding inputs, expected outputs and simulated outputs for those two cases. The source files should contain appropriate comments for better understanding.

1. Design a fully connected 3x3 reconfigurable computing architecture where each computational unit (CU) in a row can send information to any of the CUs in the row below it. For example, CU(1,1) can send information to CU(2,1), CU(2,2) and CU(2,3). Each CU can perform Arithmetic Shift Left, Arithmetic Shift Right, Rotate Shift Left, Rotate Shift Right, Logical Shift Left, Logical Shift Right operations.

* Use Xilinx Vivado to design and simulate the logic shown above.
* Inputs are 4-bit wide.
* Make sure you test your design for all the operations listed above.

Submit vhdl code, RTL schematic, screenshots of simulation waveforms, and test bench of the design. Test your design using at least five test cases. Mark two of the test cases and show the corresponding inputs, expected outputs and simulated outputs for those two cases. The source files should contain appropriate comments for better understanding.